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What if glass enables the next generation of advanced semiconductor packages?



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1. Executive summary

As conventional transistor scaling becomes harder to extend, semiconductor progress is shifting toward package- and system-level integration. Advanced packaging is therefore becoming a central performance lever, while materials play a greater role in determining how reliably complex architectures can be manufactured. Glass is gaining relevance because it can support both the structure of advanced packages and the processes needed to build them. Its future role will depend on where its material performance can be translated into reliable industrial value.

2. The shift beyond Moore's Law

For decades, semiconductor progress was shaped by a powerful scaling assumption: more performance could be achieved by placing more transistors on a chip. Gordon Moore's 1965 observation became the organizing logic behind much of the industry's innovation, investment, and manufacturing scale.[1] As long as smaller features delivered predictable gains in density, performance, and cost, transistor scaling provided a remarkably effective path forward.

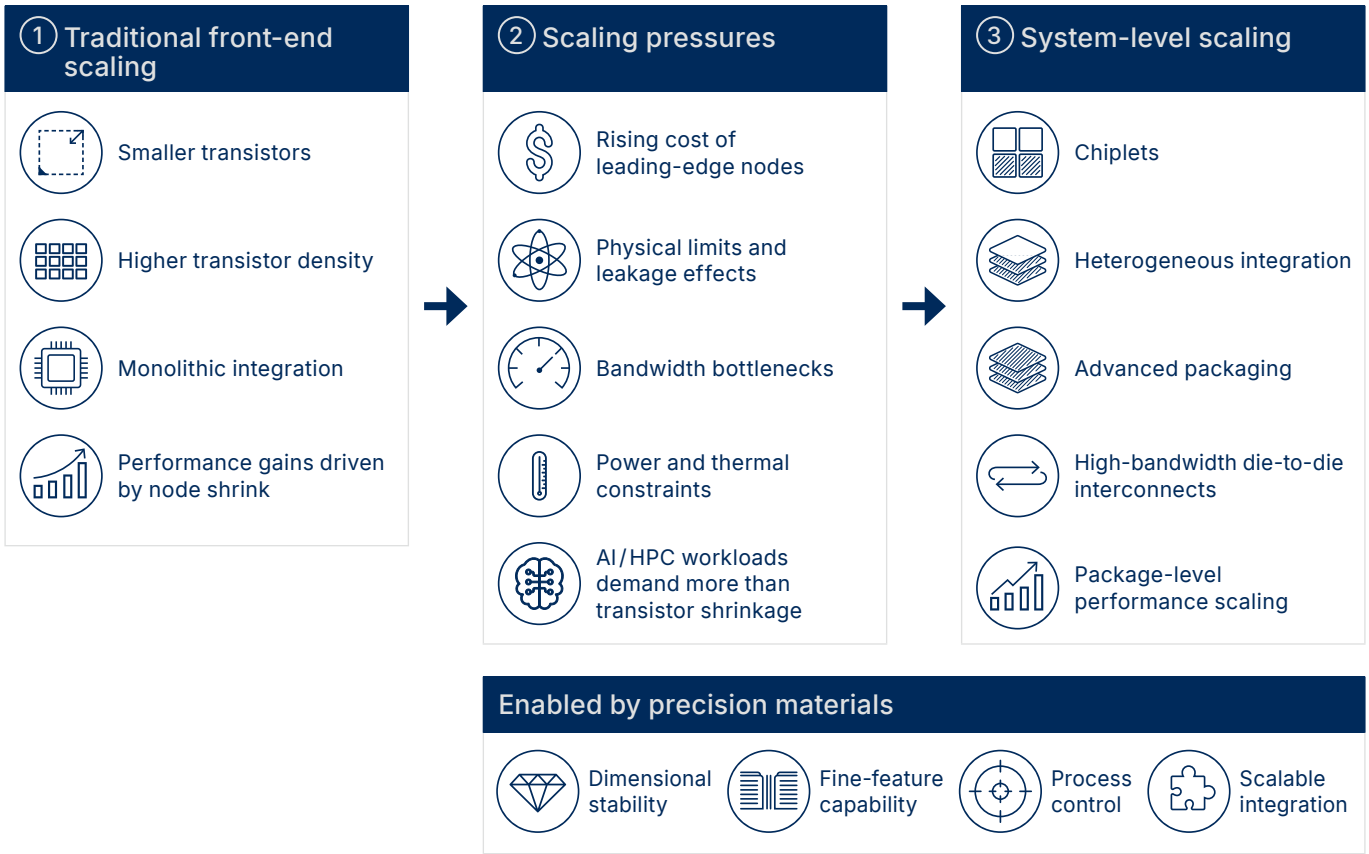
That path remains important, but it has become harder to extend. Further advances in lithography, transistor architecture, materials engineering, and process control continue, yet each generation requires greater technical effort and economic investment.[2] At very small technology nodes, physical effects such as gate oxide tunneling and source-to-drain tunneling add further pressure by increasing leakage currents and complicating performance, power, and reliability.[3]

The result is a broader definition of scaling. The industry is no longer focused solely on shrinking the individual transistor. Progress depends on how logic, memory, accelerators, and other functional elements are integrated into systems that can deliver more computational capability within realistic manufacturing and cost constraints.

Advanced packaging has therefore moved into the center of the scaling discussion. AI and high-performance computing workloads depend heavily on fast data movement, high memory bandwidth, efficient power delivery, and reliable multi-die integration. In these architectures, the package is part of the performance path. It influences how closely functional blocks can be placed, how efficiently they communicate, and how reliably the resulting system can be manufactured.[4]

This shift changes the role of packaging materials. As packages become larger, denser, and more structurally complex, mechanical and dimensional stability are no longer secondary considerations. They shape overlay accuracy, bonding quality, interconnect reliability, and yield. A package architecture can only deliver its intended performance if the materials behind it can maintain control through fabrication, assembly, and operation.

The shift beyond Moore's Law is therefore not a retreat from scaling. It is a relocation of part of the scaling challenge from the transistor alone to the package and system level. Once packaging becomes a performance lever, the material platforms behind packaging become strategic.



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